#### Education

#### University of Michigan

Bachelor of Science in Computer Science

GPA: 3.88/4.00 | Awards: James B. Angell Scholar, William J. Branstrom Prize, University Honors, Regent's Scholar
Relevant Courses: Data Structures & Algorithms, Operating Systems, Computer Architecture, Web Systems, Computer Science Theory, Intro to Computer Architecture, Discrete Math, Probability Theory, Linear Algebra

# **Technical Skills**

Languages: C, C++, Python3, ARM, RISC-V, SystemVerilog, Bash Technologies: Linux, Vim, Git, GDB, LLDB, Mercurial, QEMU, perf, Valgrind, Make, CMake

#### Experience

# Apple CoreOS

Software Development Engineer Intern

• Developing storage device drivers for macOS.

# Qumulo

Member of Technical Staff Intern

• Single-node cloud cluster infrastructure and performance, file system index object metrics, and DKV upgrade.

# Ordered Systems Lab

Research Assistant

- Wrote a program in C leveraging the liburing API to asynchronously read a file on Linux with io\_uring.
- Configured Meta's RocksDB on a Debian Linux VM using QEMU, integrating Meta's folly library for advanced C++20 features, including coroutines and asynchronous I/O. Evaluated seek and scan operations using RocksDB db\_bench.
- Conducted a comparative analysis of asynchronous  $\mathrm{I/O}$  libraries, including liburing and libaio.

#### Departmental Computing Organization

Computer Consultant

• Helped manage IT infrastructure for lab machines and two server rooms. Configured Windows 10/11, macOS, and Linux systems. Implemented network solutions using Active Directory and DNS. Provided technical support and maintained security across diverse environments. Developed skills in system administration and network management.

# Projects

#### **Out-of-Order RISC-V Processor**

- Architected a RISC-V processor using SystemVerilog featuring N-way superscalar out-of-order execution, early tag broadcast, early branch resolution, fast branch recovery, Gshare prediction, branch target buffer, non-blocking data cache, store-load forwarding, and instruction prefetching.
- Developed RTL and verification testbenches to validate system performance.

#### Thread Library

• Developed a kernel-level C++ thread library on UNIX, managing CPU booting, thread life cycle, and scheduling for multiple CPUs. Implemented synchronization primitives like spin-locks, mutexes, and condition variables using advanced UNIX context management techniques.

#### Virtual Memory Pager

• Designed and implemented a virtual memory pager supporting multiple processes with swap-backed and file-backed memory pages, akin to UNIX mmap. Handled process creation, page faults, memory management unit (MMU) bits, process forking, and destruction with copy-on-write optimization.

#### Multi-threaded Network File Server

• Built a concurrent, crash-consistent network file server, supporting multiple users with nested files and directories. Ensured crash consistency using committing writes, and optimized concurrency with Boost threads and reader-writer locks. Implemented network communication using POSIX sockets for client-server interactions.

#### Other

# Ann Arbor, MI

August 2022 - May 2026

# Seattle, WA

Cupertino, CA May 2025 - Present

January 2025 - April 2025

# University of Michigan

May 2024 - December 2024

University of Michigan

June 2022 - September 2022